REMARKS

Claims 1-4 and 7-10 are now pending in the application. Claims 5 and 6 are cancelled without disclaimer or prejudice to the subject matter contained therein. Claims 7-10 are added. While Applicant disagrees with the current rejections, Applicant has amended the claims to expedite prosecution. Applicant reserves the right to pursue the claims as originally filed in one or more continuing applications. Support for the amendments to the claims can be found throughout the drawings and specification. As such, no new matter is added. The Examiner is respectfully requested to reconsider and withdraw the rejections in view of the amendments and remarks contained herein.

REJECTION UNDER 35 U.S.C. § 103

Claims 1-5 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Mitsuida (Japanese Pub. No. 2002/064749 A) in view of Yonemoto (Japanese Pub. No. 10/200817 A). This rejection is respectfully traversed.

With respect to claim 1, Mitsuida, either singly or in combination with Yonemoto, fails to show, teach, or suggest the circuit for changing the gate-applied voltage applying a second voltage to each of the gates of the plurality of transistors in the plurality of lines while in a reset state after the accumulation state.

It is a longstanding rule that to establish a prima facie case of obviousness of a claimed invention, all of the claim limitations must be taught or suggested by the prior art. *In re Royka*, 180 USPQ 143 (CCPA 1974), see MPEP §2143.03. Furthermore, when evaluating claims for obviousness under 35 U.S.C. §103, all of the limitations must be considered and given weight. *Ex parte Grasselli*, 231 USPQ 393 (Bd. App.

1983), MPEP § 2144.03. Here, Mitsuida fails to disclose the limitation of the second voltage applied to the transistors in a reset state after the accumulation state.

As shown in an exemplary embodiment in FIG. 9 of the present application, a first voltage is applied during an accumulation state (e.g. a voltage applied to a line for clearing an image signal or a line for reading an image signal). After the accumulation state, a second voltage is applied during a reset state. For example, a reference voltage such as ground is applied during the reset state as shown in FIG. 9. A third voltage is applied after the reset state during a reading out (i.e. modulation) state. In other words, a second voltage is applied during a reset state in between the accumulation state and the reading out state.

The cited combination appears to be absent of any teaching or suggestion of this limitation. For example, the Examiner relies on FIG. 1 of Mitsuida to disclose the accumulation state and the reading out state. As shown in the relied upon FIG. 1 of Mitsuida, there does not appear to be a reset state where a second voltage is applied between the first and third voltages applied in the alleged accumulation and reading out states. Instead, a ground voltage Vpg is applied during the accumulation state. In the immediately following reading out state, the applied voltage Vpg is 2.2 volts. Accordingly, Mitsuida fails to disclose the limitation of the second voltage applied to the transistors in a reset state after the accumulation state.

In view of the foregoing, Applicant respectfully submits that claim 1, as well as its dependent claims, should be allowable for at least the above reasons.

NEW CLAIMS

Claims 7-10 are added. Claims 7-10 depend either directly or indirectly from claim 1, which Applicant believes to be allowable. Therefore, claims 7-10 should be allowable for at least similar reasons.

CONCLUSION

It is believed that all of the stated grounds of rejection have been properly traversed, accommodated, or rendered moot. Applicant therefore respectfully requests that the Examiner reconsider and withdraw all presently outstanding rejections. It is believed that a full and complete response has been made to the outstanding Office Action and the present application is in condition for allowance. Thus, prompt and favorable consideration of this amendment is respectfully requested. If the Examiner believes that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at (248) 641-1600.

Respectfully submitted,

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